AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (canceled)

2. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape provided along a side wall portion of hole in an interlayer insulating film and a bottom portion of athe hole provided in anthe interlayer insulating film, and has a bottom portion of said lower electrode having a thickness greater than a side wall portion of said lower electrode.

3. (previously presented): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape-provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film and has a thickness of 30 nm or greater at the bottom portion of said lower electrode and a thickness of less than 30 nm at a side wall portion of said lower electrode.

4. - 7. (cancelled):

8. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape provided along a side wall portion and abottom portion of a hole provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected to said second metal layer along at only an entire bottom of said lower electrode and at no other portion, to said second metal layer and said lower electrode has a thickness of 30 nm or greater at the bottom portion of said lower electrode.

9. (previously presented): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate and a

capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom of said lower electrode to said second metal layer and said lower electrode has a thickness of 30 nm or greater at the bottom portion of said lower electrode and a thickness of less than 30 nm at a side wall portion of said lower electrode.

10 - 14. (cancelled)

15. (currently amended): The semiconductor device according to any one of claims 12 and 8 through 4 and claims 8 through 10, wherein said lower electrode is a metal film.

16. (currently amended): The semiconductor device according to any one of claims 12 and 8 through 4 and claims 8 through 10, wherein said lower electrode is a ruthenium film.

17. (cancelled)

18. (currently amended): The semiconductor device according to any one of claims 2 and 81 through 4 and claims 8 through 10, wherein said capacitive insulating film is a tantalum oxide film.

19. (currently amended): The semiconductor device according to any one of claims 12and 8 through 4 and claims 8 through 10, wherein said upper electrode is a ruthenium film.

20. (currently amended): The semiconductor device according to any one of claims 12 and 8through 4 and claims 8 through 10, wherein said first metal layer is a titanium nitride film.

21-48 (cancelled)

49. (currently amended): A semiconductor MIM capacitor comprising:
a lower electrode electrically connected to a metal layer at a bottom portion of said lower electrode, said lower electrode formed on a bottom of a hole and a side wall surface of the a hole in an insulating interlayer film semiconductor substrate;
a capacitive insulating film formed on said lower electrode; and
an upper electrode formed on said capacitive insulating film,
wherein said bottom portion of said lower electrode has a thickness greater than a side wall portion of said lower electrode.

50 (previously presented): The semiconductor MIM capacitor according to claim 49, wherein said lower electrode has a cup shape.

51. (previously presented): The semiconductor MIM capacitor according to claim 49, wherein said lower electrode has thickness of 30 nm or greater at said bottom portion and a thickness of less than 30 nm at said side wall portion.

52. (previously presented): The semiconductor MIM capacitor according to claim 49, wherein the entire portion of said bottom portion of said lower electrode is connected to said metal layer.

53. (new): The semiconductor device according to claim 3, wherein said lower electrode is a metal film.

54. (new): The semiconductor device according to claim 3, wherein said lower electrode is a ruthenium film.

55. (new): The semiconductor device according to claim 3, wherein said capacitive insulating film is a tantalum oxide film.

56. (new): The semiconductor device according to claim 3, wherein said upper electrode is a ruthenium film.

57. (new): The semiconductor device according to claim 3, wherein said first metal layer is a titanium nitride film.

58. (new): The semiconductor device according to claim 9, wherein said lower electrode is a metal film.

59. (new): The semiconductor device according to claim 9, wherein said lower electrode is a ruthenium film.

60. (new): The semiconductor device according to claim 9, wherein said capacitive insulating film is a tantalum oxide film.

61. (new): The semiconductor device according to claim 9, wherein said upper electrode is a ruthenium film.

62. (new): The semiconductor device according to claim 9, wherein said first metal layer is a titanium nitride film.